1. A method for estimating burn-in time for integrated circuits comprising the steps of:

providing a substrate;

forming a plurality of testing structures on said substrate, each substrate being formed by the steps of:

forming a plurality of evaluation device structures on said substrate, each device structure created to permit evaluation of failure mechanisms of said integrated circuit,

forming a first forcing input pad to provide a first forcing stimulus to at least one of said evaluation device structures to provide a first stimulus to stress said evaluation device structure,

forming a second forcing input pad to provide a second forcing stimulus to at least one of said evaluation device structures to further stress said evaluation device structure,

forming a first sensing output pad connected to sense a first response from at least one of said evaluation device structures,

forming a second sensing output pad connected to sense a second response from at least one of said evaluation device structures, and

forming a selection circuit connected to selectively communicate the second stimulus to at least one selected evaluation device structure and the second response from the selected evaluation devices structure;

activating said first and second stimuli;

stressing said substrate;

examining each selected evaluation device structure for failure;

determining a hazard rate for each failure mechanism of said integrated circuit; and

determining a burn-in time for said integrated circuit.

2. The method of claim 1 wherein the forming of the evaluation device structure further comprises the step of:

stacking multiple evaluation device structures as they are formed at a top surface of said substrate.

3. The method of claim 1 wherein forming the selection circuit comprises the steps of:

forming a plurality of transmission MOS devices, each transmission MOS device being connected between the first stimulus input pad and one of the evaluation device structures;

forming a decoder circuit in communication with a gate terminal of each of the plurality of transmission MOS devices to activate selected transmission MOS devices to selectively connect at least one of the evaluation device structures to the first stimulus input pad; and

forming a counter circuit in communication with the decoder circuit to provide an address code indicating which of the evaluation device structures are to be selected.

4. The method of claim 3 wherein the forming the selection further comprises the step of:

forming a function control input pad to transfer an increment signal to the counter stimulating the counter to increment to modify the address code to select which of the evaluation device structures are selected.

5. The method of claim 1 wherein the evaluation device structures are selected from a group of evaluation device structures consisting of capacitor dielectric film evaluation devices, gate oxide integrity devices, polycrystalline silicon heating devices, contact metallurgy evaluation chains, interlayer via chains, MOS evaluation devices, plasma etching antenna effect patterns, metal electromigration structures, memory cell array, and specially designed circuit block structures.

6. The method of claim 1 wherein the evaluation device test structures are formed in a scribe line area between the integrated circuits on said substrate.

7. An apparatus for estimating burn-in time for integrated circuits comprising:

means for providing a substrate;

means for forming a plurality of testing structures on said substrate, said means comprising:

means for forming a plurality of evaluation device structures on said substrate, each device structure created to permit evaluation of failure mechanisms of said integrated circuit,

means for forming a first forcing input pad to provide a first forcing stimulus to at least one of said evaluation device structures to provide a first stimulus to stress said evaluation device structure,

means for forming a second forcing input pad to provide a second forcing stimulus to at least one of said evaluation device structures to provide a second stimulus to further stress said evaluation device structure,

means for forming a first sensing output pad connected to sense first response from at least one of said evaluation device structures,

means for forming a second sensing output pad connected to sense a second response from at least one of said evaluation device structures, and

means for forming a selection circuit connected to selectively communicate the second stimulus to at least one selected evaluation device structure and the second response from the selected evaluation devices structure;

means for activating said first and second stimuli;

means for stressing said substrate;

means for examining each selected evaluation device structure for failure;

means for determining a hazard rate for each failure mechanism of said integrated circuit; and

means for determining a burn-in time for said integrated circuit.

8. The apparatus of claim 7 wherein the means for forming of the evaluation device structure further comprises:

means for stacking multiple evaluation device structures as they are formed at a top surface of said substrate.

9. The apparatus of claim 7 wherein means for forming the selection circuit comprises:

means for forming a plurality of transmission MOS devices, each transmission MOS device being connected between the first stimulus input pad and one of the evaluation device structures;

means for forming a decoder circuit in communication with a gate terminal of each of the plurality of transmission MOS devices to activate selected transmission MOS devices to selectively connect at least one of the evaluation device structures to the first stimulus input pad; and

means for forming a counter circuit in communication with the decoder circuit to provide an address code indicating which of the evaluation device structures are to be selected.

10. The apparatus of claim 9 wherein the means for forming the selection further comprises:

means for forming a function control input pad to transfer an increment signal to the counter stimulating the counter to

increment to modify the address code to select which of the evaluation device structures are selected.

11. The apparatus of claim 7 wherein the evaluation device structures are selected from a group of evaluation device structures consisting of capacitor dielectric film evaluation devices, gate oxide integrity devices, polycrystalline silicon heating devices, contact metallurgy evaluation chains, interlayer via chains, MOS evaluation devices, plasma etching antenna effect patterns, metal electromigration structures, memory cell array, and specially designed circuit block structures.

12. The apparatus of claim 7 wherein the evaluation device test structures are formed in a scribe line area between the integrated circuits on said substrate

13. A reliability testing structure formed on a substrate comprising:

a plurality of evaluation device structures formed on said substrate, each device structure created to permit evaluation of one of a plurality of failure mechanisms of said integrated circuit;

a first forcing input pad to provide a first forcing stimulus to at least one of said evaluation device structures to provide a first stimulus to stress said evaluation device structure;

a second forcing input pad to provide a second forcing stimulus to at least one of said evaluation device structures to provide a second stimulus to further stress said evaluation device structure;

a first sensing output pad connected to sense first response from at least one of said evaluation device structures;

a second sensing output pad connected to sense a second response from at least one of said evaluation device structures; and

a selection circuit connected to selectively communicate the second stimulus to at least one selected evaluation device structure and the second response from the selected evaluation device structure.

14. The reliability testing structure of claim 13 wherein multiple evaluation device structures are stacked as they are formed at a top surface of said substrate.

15. The reliability testing structure of claim 13 wherein the selection circuit comprises:

a plurality of transmission MOS devices, each transmission MOS device being connected between the first stimulus input pad and one of the evaluation device structures;

a decoder circuit in communication with a gate terminal of each of the plurality of transmission MOS devices to activate selected transmission MOS devices to selectively connect at least one of the evaluation device structures to the first stimulus input pad; and

a counter circuit in communication with the decoder circuit to create from an increment signal, an address code indicating which of the evaluation device structures are to be selected.

16. The reliability testing structure of claim 15 wherein the selection circuit further comprises:

a function control input pad to transfer the increment signal to the counter stimulating the counter to increment to modify the address code to select which of the evaluation device structures are selected.

17. The reliability testing structure of claim 15 wherein the counter circuit comprises;

an adder circuit which sums a next address code with the increment signal to generate the next address code;

a first transmission gate in communication with the adder circuit to selectively transmit the next address code;

a first buffer in communication with the first transmission gate to receive and retain the next address code;

a second transmission gate in communication with the first buffer to selectively transmit the next address code from the first buffer; and

a second buffer in communication with the second transmission gate to receive, retain and then transfer to the decoder the next address code.

18. The reliability testing structure of claim 17 further comprising

a clock modulator that receives the increment signal and provides first and second increment signals to selectively activate the first and second transmission gates to transfer the next address code to the first and second buffers.

19. The reliability testing structure of claim 17 further comprising:

a first delaying circuit between the adder circuit and the first transmission gate to adjust timing of the transmitting of the next address code from the adder circuit to the first transmission gate;

a second delaying circuit between the first transmission gate and the first buffer to adjust timing of the transmitting of the next address code from the first transmission gate to the first buffer;

a third delaying circuit between the first buffer and the second transmission gate to adjust timing of the transmitting of the next address code from the first buffer to the second transmission gate; and

a fourth delaying circuit between the second transmission gate and the second buffer to adjust timing of the transmitting of the next address code from the second transmission to the second buffer;

20. The reliability testing structure of claim 17 further comprising:

an initial value circuit in communication with the first buffer and the second transmission gate to establish an initial value for said next address code.

21. The reliability structure of claim 17 wherein the adder comprises:

a first summing circuit connected to receive and add the increment signal and a least significant bit of the present address code to form a least significant bit of a next address code;

a first carry circuit connected to receive the increment signal and the least significant bit of the present address code to determine a first carry bit from the sum of the increment signal and the least significant bit of the present address code;

a plurality of summing circuits, each summing circuit connected to receive and add one of plurality of bits of the present address code and a carry bit determined from an adjacent less significant bit of the next address code to form one of a plurality of bits of the next address code; and

a plurality of carry circuits, each carry circuit connected to receive one of the plurality of bit of the present address code and the carry bit determined from the adjacent less significant bit of the present address code to form one of a plurality of carry bits.

22. The reliability testing structure of claim 21 wherein the first summing circuit and the plurality of summing circuits are exclusive-OR gates

23. The reliability testing structure of claim 22 wherein each exclusive-OR gate comprises:

a MOS transistor of a first conductivity type having a gate connected to a first input terminal and drain connected to a second input terminal;

a MOS transistor of a second conductivity type having a gate connected to a first input terminal and drain connected to a second input terminal;

a first inverter circuit having an input connected to a source of the MOS transistor of the first conductivity type and an output connected to a source of the MOS transistor of the second conductivity type;

a second inverter circuit having an input connected to the source of the MOS transistor of the second conductivity type and an output connected to the source of the MOS transistor of the first conductivity type; and

an output terminal formed at the connection of the source of the MOS transistor of the first conductivity type, the output of the first inverter circuit, and the input of the first inverter circuit.

24. The reliability testing structure of claim 21 wherein the carry circuit is an AND circuit.

25. The reliability testing structure of claim 24 wherein the AND circuit comprises:

a first MOS transistor the first conductivity type having a gate connected to a first input terminal, a source connected to an output terminal, and a drain connected to a voltage reference terminal;

a second MOS transistor of the second conductivity type a gate connected to a second input terminal, a source connected to the output terminal, and a drain connected to a voltage reference terminal; and

a first depletion MOS transistor of the second conductivity type having a gate and source connected to the output terminal and a drain connected to a voltage supply terminal.

26. The reliability testing structure of claim 18 wherein the clock modulator circuit comprises:

a resistor capacitor network connected to receive the increment signal, to slow transitions of the increment signal so as to adjust a time at which said increment signal is at an active voltage level,

a first buffering circuit connected to the resistor capacitor network to generate the first increment signal from the increment signal with the slowed transitions; and

a second buffering circuit connected to the resistor capacitor network to generate the second increment signal from the increment signal with slowed transitions.

27. The reliability testing structure of claim 20 wherein the initial value circuit comprises:

a resistor having a first terminal connected to a voltage supply terminal;

a capacitor having a first terminal connected to a second terminal of the resistor and second terminal connected to a voltage reference terminal;

a plurality of second depletion MOS transistors of the first conductivity type, each second depletion MOS transistors of the first conductivity type having a gate connected to the connection of the first terminal of the capacitor and the second terminal of the resistor, a source connected to the voltage supply terminal and a drain connected to an output of the first buffer.

28. The reliability testing structure of claim 13 wherein the evaluation device structures are selected from a group of evaluation device structures consisting of capacitor dielectric film evaluation devices, gate oxide integrity devices, polycrystalline silicon heating devices, contact metallurgy evaluation chains, interlayer via chains, MOS evaluation devices, plasma etching antenna effect patterns, metal electromigration structures, memory cell array, and specially designed circuit block structures.

29. The reliability testing structure of claim 13 wherein the evaluation device test structures are formed in a scribe line area between the integrated circuits on said substrate.

30. A reliability evaluation test structure to reduce area requirements of said test structure when formed on a substrate, comprising:

a plurality of evaluation devices formed on a surface of the substrate such that multiple evaluation devices are placed on said substrate in a stack; and

at least one input/output pad connected to said evaluation devices to communicate a stimulus to selected evaluation devices and response from said evaluation devices.

31. The reliability evaluation test structure of claim 30 wherein the evaluation devices are selected from a group of evaluation devices consisting of capacitor dielectric film evaluation devices, gate oxide integrity devices,

polycrystalline silicon heating devices, contact metallurgy evaluation chains, interlayer via chains, MOS evaluation devices, plasma etching antenna effect patterns, metal electromigration structures, memory cell array, and specially designed circuit block structures.

32. The reliability evaluation test structure of claim 30 wherein the reliability evaluation test structure is formed in a scribe line area between the integrated circuits on said substrate.

33. An integrated circuit wafer, comprising:

a substrate on to which multiple integrated circuit die are formed;

a plurality of evaluation devices formed on a surface of the substrate such that multiple evaluation devices are placed on said substrate in a stack; and

at least one input/output pad connected to said evaluation devices to communicate stimulus to selected evaluation devices and response from said evaluation devices.

34. The reliability evaluation test structure of claim 33 wherein the evaluation devices are selected from a group of evaluation devices consisting of capacitor dielectric film evaluation devices, gate oxide integrity devices, polycrystalline silicon heating devices, contact metallurgy evaluation chains, interlayer via chains, MOS evaluation devices, plasma etching

antenna effect patterns, metal electromigration structures, memory cell array, and specially designed circuit block structures.

35. The reliability evaluation test structure of claim 33 wherein the reliability evaluation test structures are formed in a scribe line area between the integrated circuit die on said substrate.

36. A method for forming a reliability testing structure on a substrate comprising the steps of:

providing a substrate;

forming a plurality of testing structures on said substrate, each testing structure being formed by the steps of:

forming a plurality of evaluation device structures on said substrate such that multiple evaluation device structures are placed on said substrate in a stack, each device structure created to permit evaluation of failure mechanisms of said integrated circuit and ,

forming a first forcing input pad to provide a first forcing stimulus to at least one of said evaluation device structures to provide a first stimulus to stress said evaluation device structure,

forming a second forcing input pad to provide a second forcing stimulus to at least one of said evaluation device structures

to provide a second stimulus to further stress said evaluation device structure,

forming a first sensing output pad connected to sense first response from at least one of said evaluation device structures,

forming a second sensing output pad connected to sense a second response from at least one of said evaluation device structures, and

forming a selection circuit connected to selectively communicate the second stimulus to at least one selected evaluation device structure and the second response from the selected evaluation devices structure;

37. The method of claim 36 wherein the evaluation devices are selected from a group of evaluation devices consisting of capacitor dielectric film evaluation devices, gate oxide integrity devices, polycrystalline silicon heating devices, contact metallurgy evaluation chains, interlayer via chains, MOS evaluation devices, plasma etching antenna effect patterns, metal electromigration structures, memory cell array, and specially designed circuit block structures.

38. The method of claim 36 wherein the reliability evaluation test structure is formed in a scribe line area between integrated circuits on said substrate.